PAPER ID-411430

Subject Code: KEE401

Roll No: | | | | | | | | | | | | | |

BTECH
(SEM IV) THEORY EXAMINATION 2023-24
DIGITAL ELECTRONICS

TIME: 3 HRS **M.MARKS: 100**

Note: 1. Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt *all* questions in brief.

Q no.	Question	Marks	CO
a.	Convert the binary number $(11001)_2$ into (i) Gray code (ii) Excess-3 Code.	2	1
b.	Compute the given subtraction using 2's complement $(100010)_2$-$(11010)_2$	2	1
c.	Show the function $A+B\bar{C}$ in canonical SOP form.	2	2
d.	Differentiate serial adder and parallel adder.	2	2
e.	The group of bits 11001 is serially shifted (right-most bit first) into a 5-bit parallel output shift-register with an initial state 01110. What is the contains After three clock pulses, the register contains	2	3
f.	Differentiate between synchronous and asynchronous counters.	2	3
g.	Explain State Reduction and assignment for synchronous sequential circuits	2	4
h.	Compare Mealy and Moore state machine.	2	4
i.	Define term power dissipation in logic families.	2	5
j.	Differentiate RAM and ROM.	2	5

SECTION B

2. Attempt any *three* of the following:

a.	Simplify the following Boolean function using K-map and also draw the simplified logic circuit using NAND gate only. $F(A,B,C,D,E)=\sum_m(0,1,2,4,7,8,12,14,15,16,17,18,20,24,28,30,31)$	10	1
b.	Implement the function $Y(A,B,C,D)=\sum_m(0,1,2,5,8,13,14)$ using 8:1 multiplexer. Consider A, B, C as the select lines.	10	2
c.	Illustrate the register with its classification and explain shift register with help of example.	10	3
d.	An asynchronous sequential circuit with two excitation function with two feedback loop is given as: $Y_1 = xy_1 + \bar{x}y_2\,; \quad Y_2 = x\bar{y}_1 + \bar{x}y_2$ Derive the transition table & obtain the flow table.	10	4
e.	Explain PLA and PAL. Implement the following Boolean function with a PLA. $F_1(x,y,z)=\sum(0,1,2,4)\,; \quad F_2(x,y,z)=\sum(0,5,6,7)$	10	5

SECTION C

3. Attempt any *one* part of the following:

a.	Simplify the following Boolean function using K-map and also draw the simplified logic circuit. $f(A,B,C,D)=\sum_m(0,1,5,6,12,13,14)+d(2,4)$	10	1
b.	Demonstrate Ex-NOR gate with the help of (i) NAND-NAND Logic only and (ii) NOR-NOR Logic gates only	10	1

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4. Attempt any *one* part of the following:

a.	Explain the design of a Full Subtractor, with its truth table and Boolean expression.	10	2
b.	Draw and Explain 2-bit magnitude comparator. Also represent output with the help of logic diagram.	10	2

5. Attempt any *one* part of the following:

a.	Express Johnson Counter with its clock sequence for unique state.	10	3
b.	Design RS flip –flop using NAND-NAND logic and obtain its characteristic equation and excitation table. Explain how will you convert it in D Flip-flop.	10	3

6. Attempt any *one* part of the following:

a.	Implement the circuit defined by the following excitation and output functions with a NOR SR Latch. Also show the implementation with NAND SR latch. $Y = x_1\bar{x}_2 + (x_1 + \bar{x}_2)y\,; \qquad z = y$	10	4
b.	Explain critical race, non-critical race conditions and race free state assignments with the help of suitable example.	10	4

7. Attempt any *one* part of the following:

a.	Explain basic structure of ECL logic family with the help of suitable example.	10	5
b.	Demonstrate universal gates using PMOS and NMOS logic family.	10	5